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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,178	11/26/2003	Hyo-Hak Nam	8071-50 (OPP 030570 US)	5722
22150	7590	06/29/2005		
F. CHAU & ASSOCIATES, LLC 130 WOODBURY ROAD WOODBURY, NY 11797			EXAMINER NGUYEN, THANH NHAN P	
			ART UNIT	PAPER NUMBER

2871

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/723,178	Applicant(s) NAM ET AL.	
	Examiner (Nancy) Thanh-Nhan P. Nguyen	Art Unit 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 01 June 2005.  
 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 17-40 is/are pending in the application.  
 4a) Of the above claim(s) 1-16 is/are withdrawn from consideration.  
 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
 6) ☒ Claim(s) 17-40 is/are rejected.  
 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☒ The drawing(s) filed on 26 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) ☒ All b) ☐ Some \* c) ☐ None of:  
 1. ☒ Certified copies of the priority documents have been received.  
 2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

1. Applicant's election with traverse of claims 17-40, corresponding to Fig. 8A in the reply filed on 6/1/2005 is acknowledged. The traversal is on the ground(s) that "applicant believes that simultaneous examination will not present an undue burden." This is not found persuasive because original claims 1-40 really contain embodiments directed to patentably distinct species (see previous Office Action dated 5/4/2005), and each species could be considered as a serious burden itself.

The requirement is still deemed proper and is therefore made FINAL.

### **Claim Rejections - 35 USC § 102**

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**Claims 17-20, and 30-31, 34-35, 37-40 are rejected under 35 U.S.C. 102(e) as being anticipated by Tashiro et al U.S. Patent Application Publication No. 2002/0196393.**

Referring to claims 17-20, Tashiro et al discloses a liquid crystal display comprising: a first panel (16) including a conductive member (78) including a light transmitting portion; a second panel (4) spaced apart from the first panel by a predetermined gap and including a black matrix (108); a sealant (6) disposed between

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the first panel and the second panel and overlapping the black matrix, the light transmitting portion disposed at the overlapping; and a liquid crystal layer (22) filled in the gap between the first panel and the second panel, and enclosed by the sealant; wherein the light transmitting portion includes at least one transparent area and at least one opaque area; wherein the at least transparent area is an opening type; and wherein the at least transparent area includes a plurality of slits or a lattice pattern, [figs. 43a-45].

Referring to claims 30-31, and 35, Tashiro et al discloses a method of manufacturing a liquid crystal display, the method comprising: forming a conductive member (78) including a light transmissive portion on a first substrate (16); forming a black matrix (108) on a second substrate (4); forming a sealant (6) overlapping the light transmissive portion; forming a liquid crystal layer (22) enclosed by the sealant; adhering the second substrate to the first substrate using the sealant; hardening the sealant to combine the first substrate and the second substrate; wherein the hardening step comprising directing light from the first substrate to the sealant to be hardened; and wherein the sealant overlaps the black matrix in part, [figs. 43a & 47a].

Referring to claim 34, Tashiro et al discloses the step of hardening comprising directing light from the first and the second substrates to the sealant to be hardened, [fig. 50].

Referring to claims 37-40, Tashiro et al discloses a liquid crystal display comprising: a first panel (16) including a conductive layer (78); a second panel (4) spaced apart from the first panel by a predetermined gap and including a black matrix

(108); a sealant (6) disposed between the first panel and the second panel and overlapping the black matrix; and a liquid crystal layer (22) filled in the gap between the first panel and the second panel and enclosed by the sealant, wherein the conductive layer has a plurality of slits located at the overlapping and elongated along a signal transmission of the conductive layer; wherein the conductive layer extends along the signal transmission; wherein the slits form at least two rows along the signal transmission; and wherein width of the slits is equal to or larger than distance between the slits, [figs. 43a-43b].

**Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tashiro et al in view of Kim et al U.S. Patent Application Publication No. 2005/0036086.**

Referring to claim 21, Tashiro et al lacks disclosure of the at least transparent area comprising a transparent conductive material. However, it was conventional to have transparent conductive material to form in transparent area, as evidenced by Kim et al, [fig. 5, transparent conductive material (24) in transparent area], and therefor had the benefits associated with being conventional, such as the benefit of being available

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and the benefit of being suitable for the intended purpose. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have the transparent area comprising a transparent conductive material for the benefit of being available and the benefit of being suitable for the intended purpose.

Referring to claim 22, Tashiro et al discloses wherein the at least transparent area occupied about 20% or more of an area occupied by the light transmitting portion, [fig. 43a].

**Claims 32-33, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tashiro et al.**

Referring to claims 32-33, Tashiro et al discloses the step of hardening comprising a reflector (152) located on the first substrate (16), [fig. 19]; directing light from the second substrate to the sealant to be hardened; wherein the light is obliquely directed to the first and the second substrates. However, Tashiro lacks disclosure of the reflector is located opposite the second substrate with respected to the first substrate. It has been determined that the arrangement of parts is within the ordinary level of skill, [MPEP 2144.04 VI (C)]. Further, disposing the reflector on the first substrate is really for the purpose of the light reflected to the sealant (6) to be hardened. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to place the reflector located opposite the second substrate with respected to the first substrate for the benefit of having light reflected to the sealant to be hardened.

Similarly, referring to claim 36, Tashiro et al lacks disclosure of the step of hardening comprising reversing relative positions of the first and second substrates before the direction of light. It has been determined that the arrangement of parts is within the ordinary level of skill, [MPEP 2144.04 VI (C)]. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to reverse relative positions of the first and second substrates before the direction of light is for the same purpose of hardening the sealant.

**Claims 23-24, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tashiro et al in view of Fukami et al U.S. Patent No. 6,816,208.**

Referring to claims 23-24, Tashiro et al lacks disclosure of the first panel further comprises a plurality of pixel electrodes and a plurality of storage electrode lines overlapping the pixel electrodes; and the second panel further comprises a common electrode.

It was well known to have common electrodes and pixel electrodes to drive the liquid crystal display panel; and to have storage electrode lines overlapping the pixel electrodes to form additional storage capacitance, as evidenced by Fukami et al, [figs. 1-2]. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a plurality of pixel electrodes and a plurality of storage electrode lines overlapping the pixel electrodes for forming additional storage capacitance; and to have common electrodes and pixel electrodes to drive the liquid crystal display panel.

Referring to claim 29, Tashiro et al discloses the conductive member (78) located out of the sealant (6), [fig. 43a]; Tashiro et al lacks discloses of the second panel comprising the common electrode. As discussed above, this limitation would be met by claims 23-24.

**Claims 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tashiro et al in view of Moon U.S. Patent Application Publication No. 2003/0067428.**

Referring to claim 25, even though Tashiro et al lacks disclosure of a gate PCB and a data PCB for supplying signals to the first and the second panels, it was well known to have a gate PCB (4) and a data PCB (6) for supplying signals to the first and the second panels, as evidenced by Moon, [fig. 1]. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a gate PCB and a data PCB for supplying signals to the first and the second panels.

Similarly, referring to claim 26, even though Tashiro et al lacks disclosure of a gate driver, wherein the first panel further comprises a plurality of thin film transistors controlled by the gate driver, it was well known to have a gate driver (12), wherein the a plurality of thin film transistors controlled by the gate driver since a gate terminal of the thin film transistor is connected to any one of the gate lines, thereby allowing a pixel voltage signal to be applied to pixel electrodes in each line, as evidenced by Moon, [fig. 1 & par. 0006]. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a gate driver, wherein the a



plurality of thin film transistors controlled by the gate driver for allowing a pixel voltage signal to be applied to pixel electrodes in each line.

Similarly, referring to claim 27, even though Tashiro et al lacks disclosure of a data driver, wherein the first panel further comprises a plurality of pixel electrodes supplied with voltages from the data driver, it was well known to have a data driver (8), wherein a plurality of pixel electrodes supplied with voltages from the data driver since each of the pixel electrodes is connected to any one of the data lines through source and drain terminals of a thin film transistor, and either the source or the drain terminals of a thin film transistor is connected to the data line, which received the voltage from the data driver, as evidenced by Moon, [fig. 1]. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a data driver, and a plurality of pixel electrodes supplied with voltages from the data driver for driving the display panel.

Claim 28 is met the discussion regarding claims 25-27 rejection above.

### **Conclusion**

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tashiro et al U.S. Patent Application Publication No. 2002/0196393.

Kim et al U.S. Patent Application Publication No. 2005/0036086.

Fukami et al U.S. Patent No. 6,816,208.

Moon U.S. Patent Application Publication No. 2003/0067428.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to (Nancy) Thanh-Nhan P. Nguyen whose telephone number is 571-272-1673. The examiner can normally be reached on M-F/9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 24, 2005

TN



**DUNG T. NGUYEN**  
**PRIMARY EXAMINER**